minus

board v1.1 (minUS_08112026)

Single-channel, USB-powered pulse-echo ultrasound front end with 3-level 5 V pulser, switchable 0–42 dB receive chain and 12-bit 25 Msps acquisition

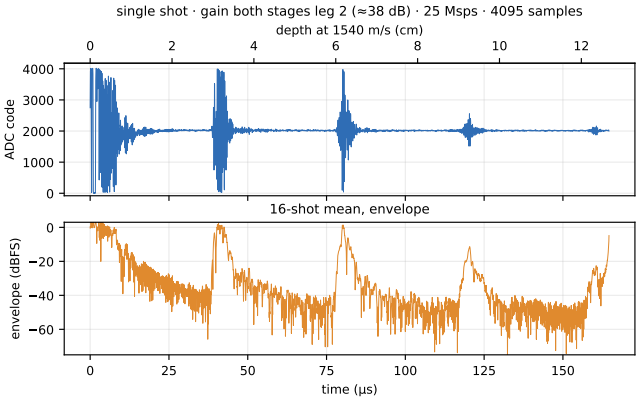
Features

- One transmit / one receive channel for a single-element piezo transducer
- **3-level pulser**: +5 V, active GND clamp, high-impedance; phase lengths programmable in 6.67 ns steps (default 200 ns / 27 ns / 500 ns)
- Pulser fires on the ADC start edge: main bang within the first sample (< 40 ns)[M]
- **Receive chain**: 24 dB wideband MMIC LNA (BGA2817) + two on-chip op-amp stages, 9 gain settings from **0 to 42.5 dB**[M]
- **12-bit ADC** at **24.86 Msps**[M], 4095 samples = 164.7 µs = 12.7 cm depth at 1540 m/s
- ADC alone: 10.5 noise-limited bits[M]; in-band input noise 13 nV/$\sqrt{\text{Hz}}$ at the OA1 input at full gain[M]
- On-chip fixed-pattern correction (period-4 pin pattern removed, `pc`)
- Two MCUs: RP2354A (USB, control, pulser PIO) + PIC32AK1216GC41048 (op-amps, ADC, DMA)
- USB-C powered and controlled (CDC console, text commands); in-system programming of the PIC by the RP
- 85.7 × 54.0 mm, 4-layer, 1.6 mm; SMA + U.FL on TX and RX

Applications

- A-mode ultrasound, time-of-flight and thickness gauging
- Teaching and experimenting with ultrasound physics and signal chains
- Liquid-level, distance and material echo measurements in the 1–5 MHz range
- Low-cost open-hardware imaging research (single element, mechanically scanned)

Typical result



Single shot and 16-shot envelope, 3.3 MHz piezo; echo train every 39.7 µs (30.6 mm one way).

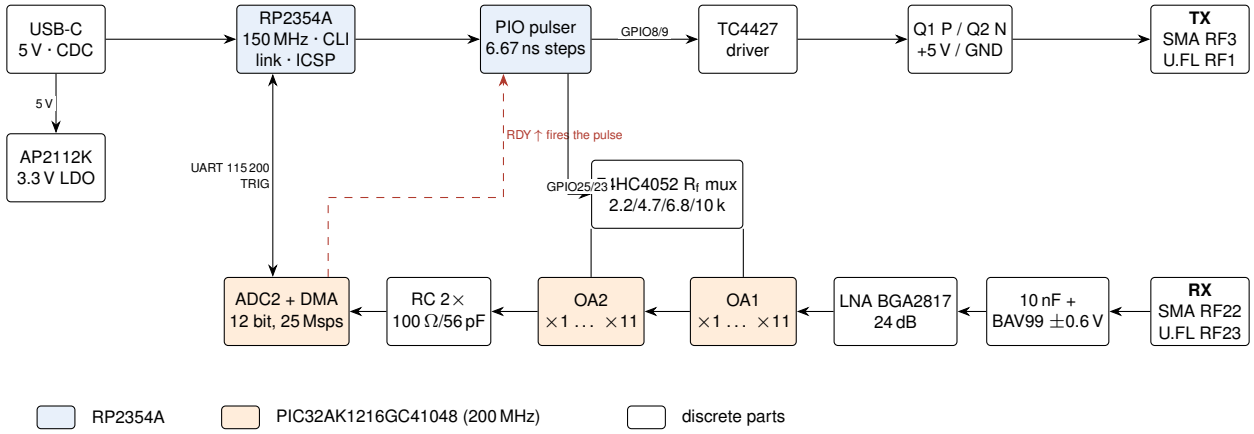


Figure 1: Block diagram. The RP2354A owns USB, the command line, the pulser and the gain mux; the PIC32AK owns the two op-amp gain stages, the ADC and the DMA capture.

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How to read this datasheet

Values marked [M] were measured on one board (RP2354A unique ID 7D4466C63B374C98, firmware rp 0.1.34 / pic 0.1.25, link protocol 10; the released firmware rp 1.1.2 / pic 1.1.0 has the same acquisition code, plus the LP5562 LED driver and new names) with a 3.3 MHz single-element piezo transducer connected (characterised in Annex 11), at room temperature, powered from a PC USB port. Values marked [D] come from the schematic, the component datasheets or the firmware and were not independently measured. Every measurement can be reproduced with the scripts in `docs/bench/2026-11-19-*/` of the repository (github.com/kelu124/minus); the raw captures are stored next to them. There is a single unit: no min/max over production is available.

1 Absolute maximum ratings and operating conditions

Parameter	Rating	Unit	Limited by
USB VBUS (+5.0 V rail)	6.0	V	AP2112K V_{IN} max 6.5 V; TC4427 VDD 18 V; IRLML2244 V_{DS} −20 V [D]
TX connector (net `Transducer`), externally applied	−0.3 … 5.3	V	Q1/Q2 body diodes to +5 V / GND [D]
RX connector (net `TRANSDUCER`), DC	±50	V	C45 10 nF series capacitor rating (0402, 50 V) [D]
RX connector, transient after C45	clamped ±0.6	V	D2 BAV99 to GND (215 mA, 4 A surge) [D]
ADC node, test points H6, J1, J2	−0.3 … AVDD+0.3	V	PIC32AK pins; D1 BAT54S on the ADC node [D]
Storage temperature	−40 … +85	°C	components [D]

Recommended operating condition	Min	Typ	Max	Unit	Notes
Supply (USB-C VBUS)	4.75	5.0	5.25	V	USB 2.0 port; also on CN1.33, H6.18 [D]
Logic / analog rails		3.3		V	AP2112K (600 mA) → DVDD, ferrite L2 → AVDD [D]
AVDD (ADC full scale)		3.32		V	from the 0.8 V band gap [M]
Ambient temperature	0	25	70	°C	all parts are industrial grade; characterised at 25 °C only
Transducer	1	3.3	7	MHz	receive chain −6 dB band set by the transducer; anti-alias 10.6 MHz [D]

2 Electrical characteristics

Unless noted: USB 5 V, 25 °C, firmware defaults (`pe 200 500 25`, ADC trigger divider 4, single conversions, pattern correction on).

Parameter	Conditions	Min	Typ	Max	Unit
Transmit (pulser)					
Output levels	no load		0 / 5.0		V [D]
Output states			+5 V, GND clamp, Hi-Z		[D]
+5 V phase t_{hi}	programmable, default 200 ns	13.3	200	27 300	ns [D]
Dead time (both FETs off)	programmable, default	26.7	26.7	873	ns [D]
GND clamp phase t_{lo}	programmable, default 500 ns	13.3	500	27 300	ns [D]
Timing resolution	PIO clock = clk_sys 150 MHz		6.67		ns [D]
Driver	TC4427 (MIC4427 alt.), 1.5 A peak, 10 Ω gate R				[D]
Switches	Q1 IRLML2244 (P), Q2 IRLML6244 (N)				[D]
Pulse to ADC start	main bang onset, all inputs		< 40		ns [M]
Sample-comb phase vs pulse	400 shots, main-bang fit, near-uniform over 1 sample		39 / 11.3		ns p-p / rms [M]
Whole-sample comb slips	echo at 37 µs / 76 µs, shots off by ±1 sample		14 / 31		% [M]
Pulse-width optimum	max. echo amplitude, 3.3 MHz probe	75	113	130	ns [M]
Effective pulse length	t_{hi} + offset (fit, incl. dead time)		+48		ns [M]
Dead zone (ring-down > 6 σ)	any t_{lo} 0–2 µs, gain 0 1 0		8.2		µs [M]
Receive chain					
Input coupling	C45 + C3 = 5 nF series, BAV99 ±0.6 V clamp				[D]
Input termination	R17 after the LNA		51		Ω [D]
LNA gain	BGA2817, specified at ≥ 250 MHz		24		dB [D]
Op-amp stage gain (each)	1 + R_f/1 kΩ, R_f 2.2/4.7/6.8/10 k	3.2		11.0	V/V [D]
OA1 measured gain	legs 0…3	3.6		10.2	V/V [M]
OA2 measured gain	legs 0…3	3.7		13.1	V/V [M]
Unity setting (UGE)	per stage		1.00		V/V [D]
Total programmable gain	9 settings, `gain leg u1 u2`	0		42.5	dB [M]
Anti-alias filter	2-pole RC, 2 × (100 Ω, 56 pF)		10.6		MHz [D]
Echo centre frequency	3.3 MHz probe, echo 1		3.22		MHz [M]

Parameter	Conditions	Min	Typ	Max	Unit
Echo −6 dB band	3.3 MHz probe	2.88		3.55	MHz [M]
Echo −6 dB envelope length	⇒ axial resolution 0.59 mm		764		ns [M]
ADC and acquisition					
Resolution			12		bit [D]
Full scale	= AVDD		3.32		V [M]
LSB			0.81		mV [M]
Sample rate	divider 4 (default)		24.87		Msps [M]
	divider 10 / 20 / 40		19.89 / 9.94 / 4.97		Msps [M]
Sample-rate tolerance	PIC FRC 8 MHz	−1.5		+1.5	% [D]
Record length			4095		samples [D]
Record duration	default		164.6		µs [M]
ADC noise alone	internal band gap, SAMC 3		0.81		LSB rms [M]
ADC noise-limited ENOB	full Nyquist band		10.5		bit [M]
ENOB (datasheet, 1 kHz sine)	DS70005592 AD34		10.5		bit [D]
Fixed pattern (period 4)	before correction / after		10.5 / 0.17		LSB rms [M]
System noise (ADC node, no pulse, transducer connected, correction on)					
Output noise, unity gain	full band / 1.5–5 MHz		3.5 / 0.44		LSB rms [M]
Noise-limited ENOB, unity	full band / 1.5–5 MHz		8.4 / 11.4		bit [M]
Output noise, 42.5 dB	full band / 1.5–5 MHz		14.5 / 4.0		LSB rms [M]
Input noise density, 42.5 dB	at OA1 input, 1.5–5 MHz		13		nV/$\sqrt{\text{Hz}}$ [M]
In-band dynamic range, 42.5 dB	full-scale sine / noise		51		dB [M]
Repeatability and throughput					
Echo amplitude repeatability	16 shots, echo 3, gain 2 0 0		2.9		% CV [M]
Echo arrival jitter	16 shots, cross-correlation		11.3		ns rms [M]
Averaging gain	8 shots, aligned, host-side		11.6		dB [M]
Time per `pe` (end to end)	incl. 8190 B at 115 200 Bd (0.71 s)		0.88		s [M]
Captures needing a re-shot	ADC 40/60/60 ns lock, build dependent	0		50	% [M]
Link and control					
USB	full speed, CDC-ACM		12		Mbit/s [D]
RP↔PIC link	UART 8N1		115 200		Bd [D]
Ping round trip	`ping`, mean of 20		1308		µs [M]

3 Typical performance characteristics

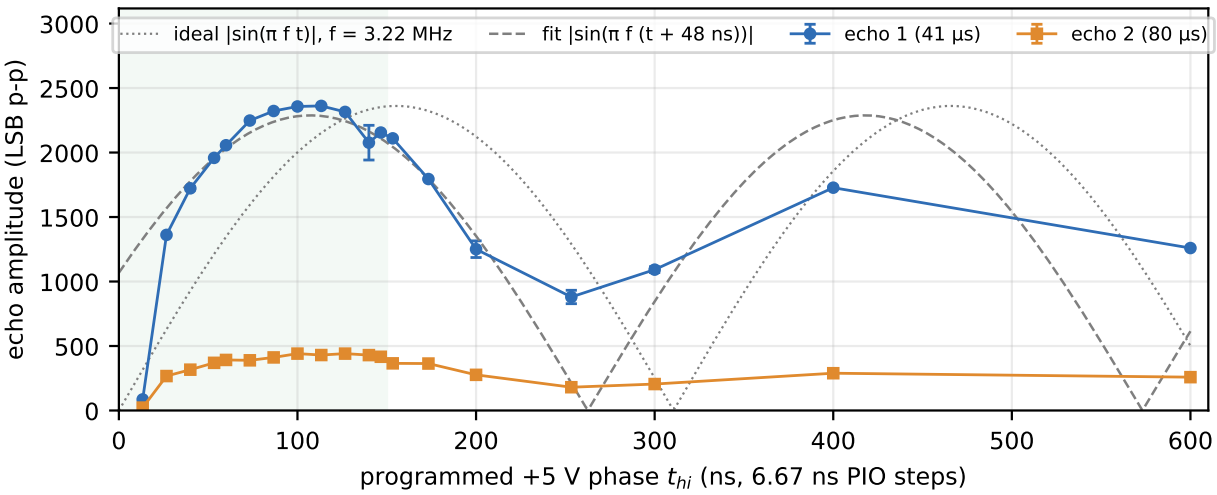
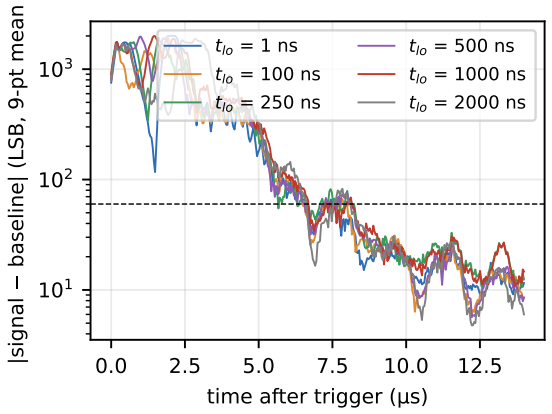
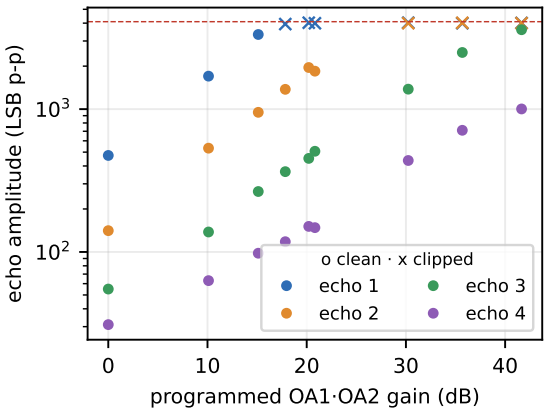


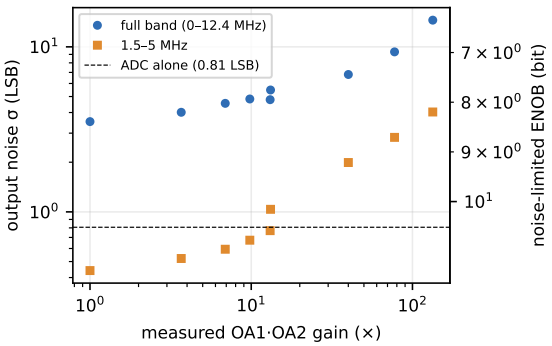
Figure 2: Echo amplitude vs +5 V phase length (gain 0 1 0, t_{lo} = 500 ns, mean of 2 shots, bars = half range)[M]. 12 points between 0 and 150 ns (shaded). Dashed: spectrum of an ideal unipolar pulse at the echo centre frequency, $|\sin(\pi f_c t_{hi})|$.



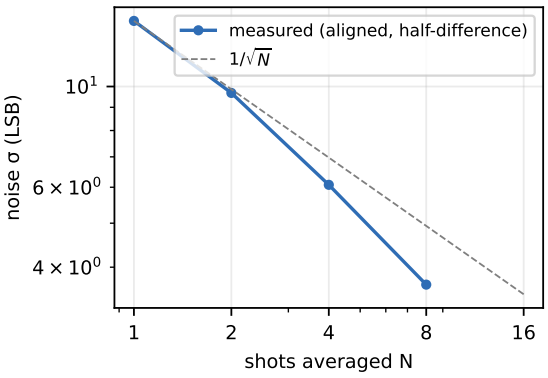
(a) Ring-down after the pulse vs GND clamp length.



(b) Echo amplitude vs programmed gain (4 echoes).



(c) Output noise and noise-limited ENOB vs gain.



(d) Noise between the echoes vs number of aligned, averaged shots (gain 2 0 0).

Figure 3: Pulser, gain and noise characteristics[M]. Echo amplitudes are peak-to-peak ADC codes at the ADC node (input 25), × = clipped. Noise = standard deviation of a pulse-free record after the firmware pattern correction; noise-limited ENOB = $12 - \log_2(\sigma\sqrt{12})$, distortion not included (upper bound).

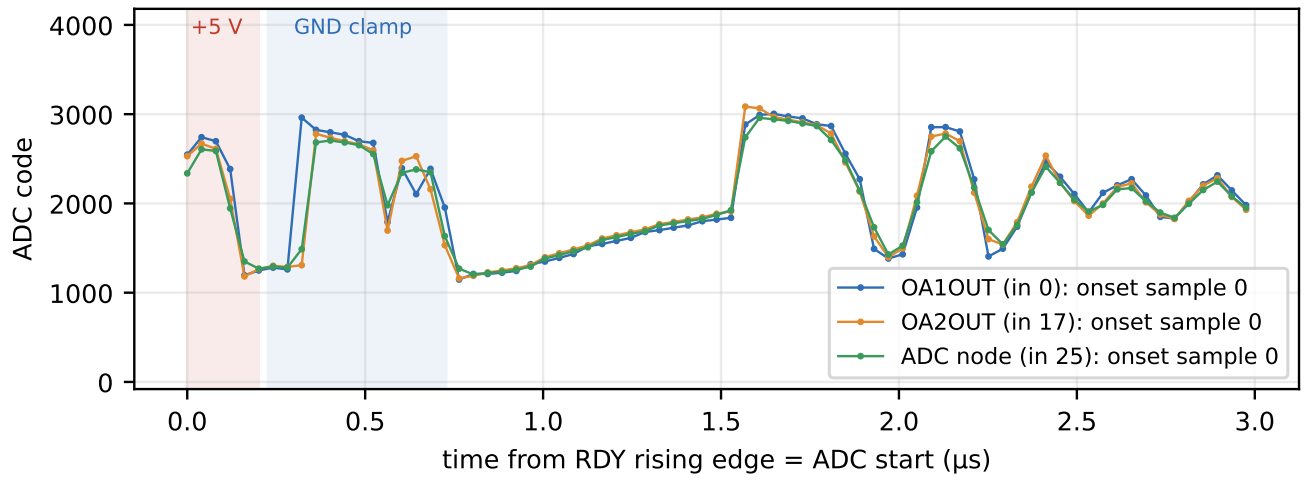


Figure 4: Main bang at unity gain on three ADC inputs, aligned on the ADC start (RDY rising edge)[M]. The shaded areas are the programmed pulse phases.

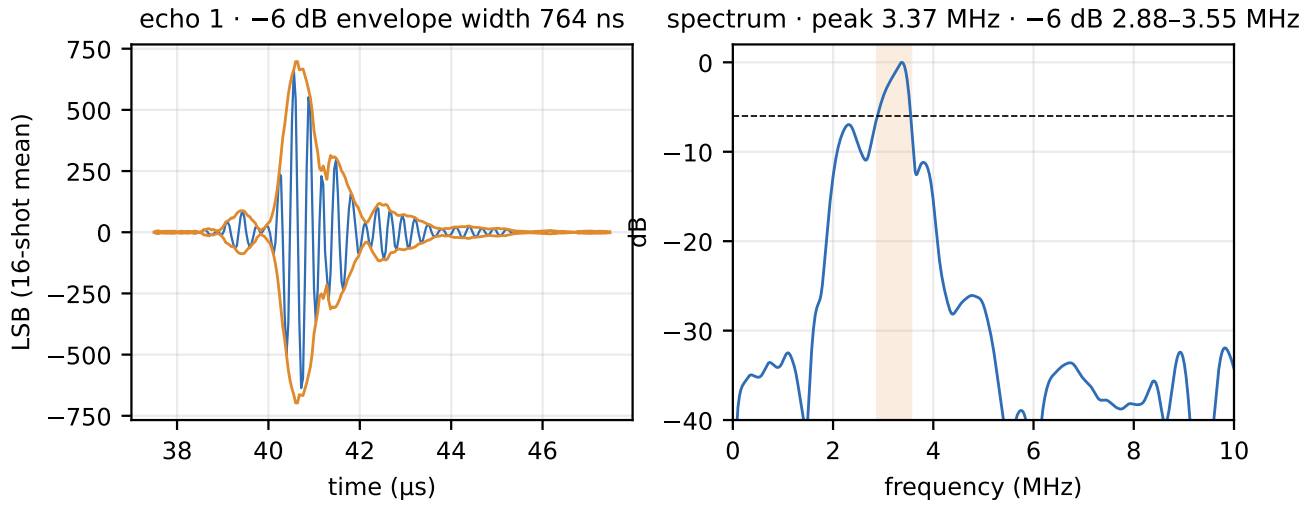


Figure 5: First echo (16-shot mean, gain 0 1 0): waveform with envelope and spectrum[M].

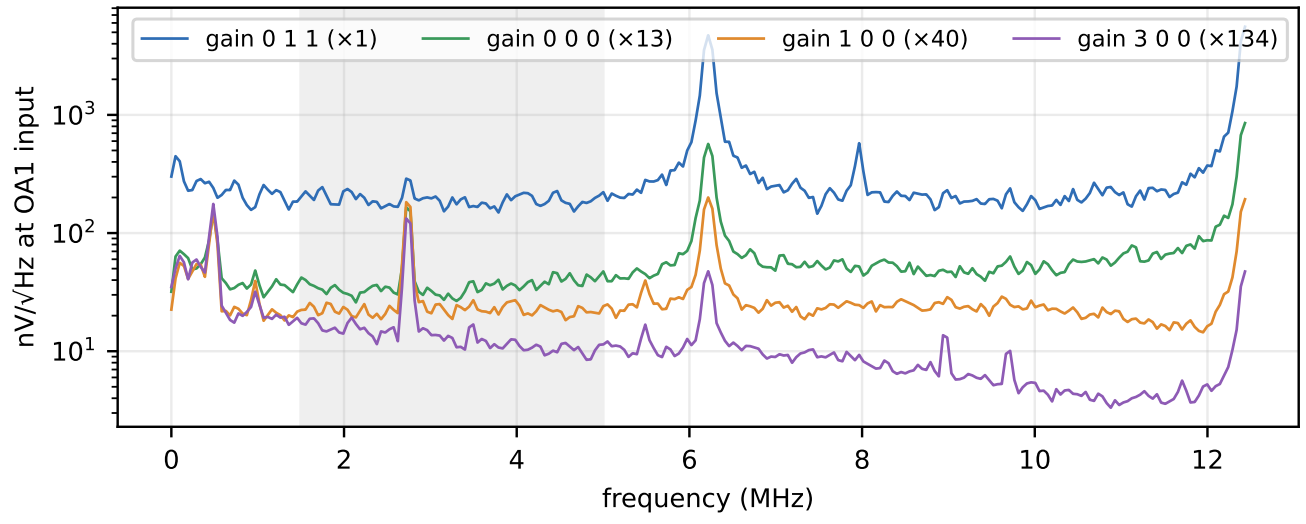


Figure 6: Noise density referred to the OA1 input (LNA output) at four gains[M]; shaded: 1.5–5 MHz. Lines at 2.72 MHz and 0.49 MHz enter at the front end; fs/4 and fs/2 residues remain at 6.21 and 12.43 MHz.

4 Functional description

4.1 Power

USB-C VBUS is the +5.0 V rail (CC pins with 5.1 kΩ pull-downs: sink only). It feeds the pulser driver and FETs directly and the AP2112K-3.3 LDO, which makes +3V3_DVDD; a 120 Ω ferrite bead (L2) derives +3V3_AVDD for the LNA, the op-amp bias dividers, the gain mux and the PIC analog supply. The RP2354A's internal switching regulator makes its 1.1 V core (L1 3.3 µH). Supply current was not measured (no meter in the loop); the LNA alone takes 20 mA[D].

4.2 Clocks

- RP2354A: 12 MHz oscillator U7 → clk_sys 150 MHz (pico-sdk 2.1.0 default). The pulser PIO runs at clk_sys: 6.67 ns steps.
- PIC32AK: internal 8 MHz FRC (±1.5 %) → PLL1 VCO 1000 MHz → 200 MHz CPU (CLKGEN1), 250 MHz ADC clock (CLKGEN6, T_{AD} 16 ns), 200 MHz SCCP time base (CLKGEN12, 5 ns).
- OSC1 32.768 kHz feeds the LP5562 LED driver only (the firmware selects the LP5562 internal clock instead).

4.3 Pulser

Two RP GPIOs drive the dual non-inverting driver U3, which drives a complementary totem on the `Transducer` net:

GPIO8 ("PWM_H")	GPIO9 ("PWM_L")	FETs	TX output
0	1	both off	released (Hi-Z), idle
0	0	Q1 (P) on	+5 V
1	1	Q2 (N) on	GND clamp
1	0	both on	shoot-through — never generated

The sequence is produced by a PIO state machine (`firmware/rp2354/pulser.pio`) from one 32-bit word per shot, so it is cycle-exact and independent of the CPU. Phase lengths: +5 V = t_{hi}, both off = dead time (≥ 4 cycles = 26.7 ns), GND = t_{lo}, then released. In pulse-echo mode the state machine waits for RDY low then high; the PIC raises RDY one instruction before starting the ADC trigger timer, so the pulse and sample 0 coincide to within a few tens of ns (< 40 ns measured).

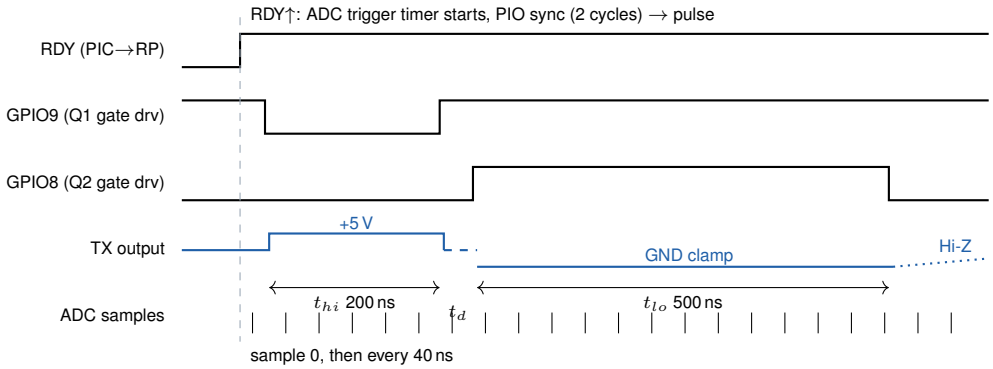


Figure 7: Pulse-echo timing (not to scale). Driver propagation (TC4427 ≈ 20 ns) and the PIO input synchroniser add a fixed delay.

4.4 Receive chain

1. **Protection and coupling**: C45 10 nF in series (blocks DC on a shared TX/RX cable), D2 BAV99 anti-parallel to GND (±0.6 V), C3 10 nF into the LNA.
2. **LNA**: BGA2817 wideband MMIC, 24 dB at RF; C32 10 nF, D3 BAV99 clamp, 51 Ω termination R17 to GND, R29 0 Ω.
3. **OA1**: PIC op amp 1, non-inverting, IN+ biased at AVDD/2 by R33/R34 through R37 (C40 330 pF coupling), R_g = R28 1 kΩ + C43 100 nF to GND (unity DC gain), R_f via 74HC4052 section 1.
4. **OA2**: identical (C1 330 pF, R31/R32/R38 bias, R30 + C44, 74HC4052 section 2).
5. **Anti-alias**: R67/C86 + R68/C87 (100 Ω/56 pF each), D1 BAT54S clamp to GND/AVDD, into AD2AN9 (pin 4).

Table 2: Gain settings (`gain <leg> <u1> <u2>`). Programmed = 1 + R_f/R_g; measured from echo ratios[M].

Command	R_f	OA1	OA2	Programmed dB	Measured dB	Noise
`gain 0 1 1`	—	×1	×1	0.0	0.0	Table 3
`gain 0 1 0`	2.2 k	×1	×3.2	10.1	11.3	
`gain 1 1 0`	4.7 k	×1	×5.7	15.1	16.8	
`gain 2 1 0`	6.8 k	×1	×7.8	17.8	19.8	
`gain 3 1 0`	10 k	×1	×11	20.8	22.3	
`gain 0 0 0`	2.2 k	×3.2	×3.2	20.2	22.4	
`gain 1 0 0`	4.7 k	×5.7	×5.7	30.2	32.0	
`gain 2 0 0`	6.8 k	×7.8	×7.8	35.7	37.8	
`gain 3 0 0`	10 k	×11	×11	41.7	42.5	

Both 4052 sections share the select lines, so OA1 and OA2 always use the same R_f leg; a stage is bypassed (×1) with the op-amp's internal unity-gain switch (AMPxCON1.UGE). The LNA gain (24 dB, not measured at 3 MHz) comes on top.

4.5 Acquisition

SCCP1 produces a 20 ns trigger comb (CLKGEN12 / 4); the 32 ns ADC2 conversion takes every second trigger, giving a uniform 40 ns sample period (24.86 Msps measured against the PIC's own timer). DMA0 moves each 16-bit result to RAM (40 ns per transfer at 200 MHz is the DMA ceiling). At some start phases the ADC locks to a 40/60/60 ns pattern (fill 226 µs instead of 164.7 µs); since pic 0.1.25 the PIC flags it (status `slow`, no payload) and `pe`/`acq` re-fire within milliseconds. How often it happens depends on the code timing of the build (0 of 12 captures with rp 0.1.34/pic 0.1.25, 0 of 400 with rp 1.1.2/pic 1.1.0, up to 50 % with earlier builds). The phase of the sample comb relative to the pulse varies from shot to shot over one full sample period: see §4.6. Align shots (cross-correlation on a strong echo, sub-sample shift) before averaging. After the capture the PIC removes the period-4 fixed pattern (below) and sends a header line plus 8190 bytes (little-endian u16) to the RP, which prints decimal samples on the USB console.

4.6 Sample-comb phase and slips (E3)

A campaign of 400 `pe` shots (`docs/bench/2026-11-19-jitter/`, rp 1.1.2/pic 1.1.0, gain 2 0 0) measured the pulse time φ against the sample comb in each shot. The main bang is purely electrical, so it was used for this: the 400 shots sample it at different phases, which gives a 1 ns equivalent-time template, and each shot's φ is a least-squares fit to it (a fit one sample away is $\sim 10^4\times$ worse, so there is no wrap ambiguity).

- φ spans 39 ns (one 40.2 ns sample), 11.3 ns rms (uniform: 11.6 ns). It is close to uniform, but not exactly (KS distance 0.09, p = 0.003): the histogram has some clustering (periodogram peak 0.27 at 4.2 ns, near the 4 ns period of the 250 MHz ADC clock).
- Shots are independent: lag-1 autocorrelation -0.03. A random 0–50 ms pause before each shot changes nothing.
- **Whole-sample slips.** Compared with φ, the strong echo at 37 µs is off by exactly ±1 sample in 14 % of shots, and the echo at 76 µs in 31 %. So during a capture the comb sometimes gains or loses a whole 40 ns period, more often the longer the capture runs. This is not visible in the fill time, whose resolution is 80 ns. The slipped shots cluster at particular start phases ($\varphi \approx -10$ and $+12$ ns), which points at a marginal trigger/conversion lock at those phases: the same mechanism as the 40/60/60 ns slow lock (E2), in a milder form. Aligned shots agree with φ to 8.1 ns rms.

Consequence for averaging: align each shot on the echo of interest, not on the main bang, and reject shots whose late echoes disagree by a whole sample. Firmware fix (not done): start the SCCP1 trigger from the ADC clock domain, or time-stamp every conversion.

4.7 Fixed-pattern correction

All external ADC inputs show a pattern locked to the sample clock with a period of four samples (one sample in four ≈ 23 LSB low, ≈ 10.5 LSB rms), independent of the analog gain; the internal band-gap input does not. It is the fs/4 and fs/2 line pair of the raw spectrum. Firmware pic 0.1.24 estimates the four phase offsets from each capture (samples 64. . . 4094, mean per phase minus overall mean, 1/16 LSB) and subtracts them. At unity gain this lowers the output noise from 8.9 to 3.6 LSB rms; the residual pattern is 0.17 LSB rms. `pc 0` disables it, `pc` shows the last offsets.

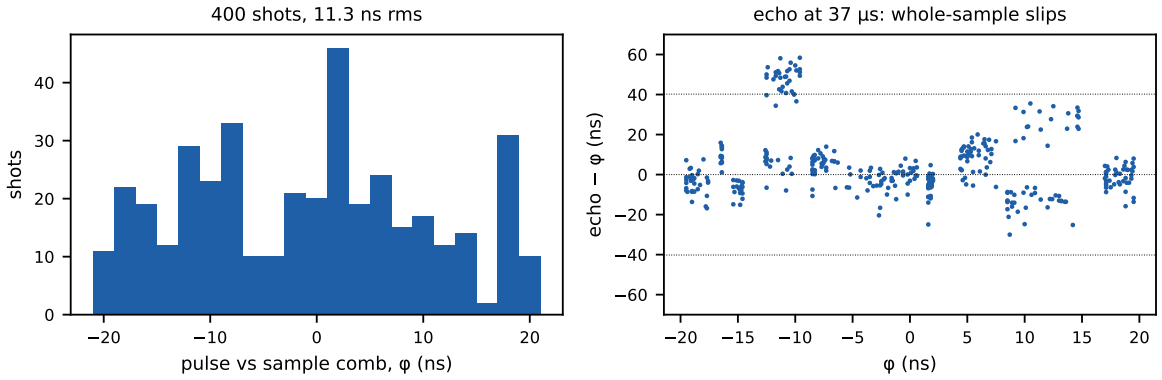


Figure 8: Left: pulse vs sample-comb phase over 400 shots. Right: echo delay minus φ (slow acoustic drift removed); bands at ± 40.2 ns are whole-sample slips.

4.8 Noise summary

Table 3: Output noise at the ADC node vs gain (firmware correction on, no pulse)[M]. Band = 1.5–5 MHz with the 2.72 MHz line notched; e_n referred to the OA1 input (= LNA output) using the measured gain.

Setting	Prog.	Meas.	Full band		1.5–5 MHz		e_n @ OA1 in
	dB	dB	LSB	ENOB	LSB	ENOB	nV/$\sqrt{\text{Hz}}$
`gain 0 1 1`	0.0	0.0	3.52	8.4	0.44	11.4	191
`gain 0 1 0`	10.1	11.3	4.01	8.2	0.52	11.1	61
`gain 1 1 0`	15.1	16.8	4.55	8.0	0.59	11.0	37
`gain 2 1 0`	17.8	19.8	4.83	7.9	0.67	10.8	30
`gain 3 1 0`	20.8	22.3	4.79	7.9	0.77	10.6	25
`gain 0 0 0`	20.2	22.4	5.48	7.8	1.04	10.2	34
`gain 1 0 0`	30.2	32.0	6.80	7.4	1.99	9.2	22
`gain 2 0 0`	35.7	37.8	9.32	7.0	2.83	8.7	16
`gain 3 0 0`	41.7	42.5	14.51	6.3	4.03	8.2	13

Below ≈ 20 dB the ADC itself sets the in-band floor; above ≈ 32 dB the front end dominates. At full gain the in-band noise referred to the LNA input is ≈ 0.85 nV/$\sqrt{\text{Hz}}$ if the LNA gives 24 dB — the thermal noise of 50 Ω (0.91 nV/$\sqrt{\text{Hz}}$) — so extra analog gain mostly amplifies front-end noise; averaging is the better lever.

5 Connectors and pin assignment

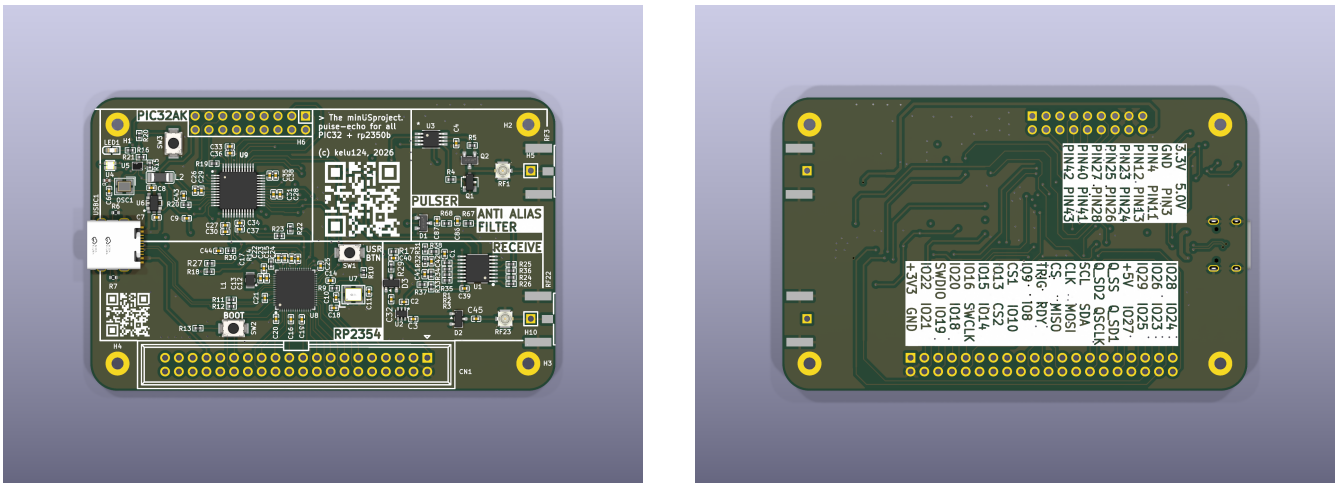


Figure 9: Top and bottom (renders from the KiCad design; 2×N headers and SMA bodies omitted).

Ref	Type	Function
USBC1	USB-C receptacle	5 V power and USB 2.0 FS (CDC console). Sink only (CC 5.1 kΩ).
RF3 / RF1 / H5	SMA / U.FL / pin	**TX**: pulser output, net `Transducer` (Q1/Q2 drains).
RF22 / RF23 / H10	SMA / U.FL / pin	**RX**: receive input, net `TRANSDUCER` (C45 series). Join TX and RX with a tee/cable for a single-element probe.
J1	1×3 socket	1 OA1IN+ (LNA out, biased AVDD/2), 2 OA1IN−, 3 OA1OUT — probe points.
J2	1×3 socket	1 OA2IN+, 2 OA2OUT, 3 OA2IN−.
H6	2×9 header	1 PIC RD6/ASDA1 · 2 SCL · 3 PIC RD3/TDI · 4 PIC RD5/ASCL1 · 5 PIC OSCO · 6 PIC OSCI · 7 UART_TX · 8 UART_RX · 9 AD1AN8 · 10 AD2AN8 · 11 OA3IN− · 12 OA3IN+ · 13 **ADC node (PIC32_ADC)** · 14 OA3OUT · 15 GND · 16 PIC PGC2/DACOUT1 · 17 +3.3 V · 18 +5 V.
CN1	2×20 IDC	RP2354A breakout: 1 +3.3 V, 2 GND, 3/4 GPIO22/21 (PIC PGD1/PGC1), 5 SWDIO, 10 SWCLK, 6–8 GPIO19/20/18, 9 UART_TX, 11/12 GPIO15/14, 13 GPIO13 PWM, 14/15 SPI_CS2/CS1, 16 GPIO10, 17/18 pulser GPIO9/8, 19 TRIG, 20 RDY, 21–24 SPI CS/MISO/CLK/MOSI, 25/26 SCL/SDA, 27–32 QSPI, 33 +5 V, 34/35/37/39 GPIO27/29/26/28, 36/38 gain mux S0/S1 (GPIO25/23), 40 GPIO24 (PIC MCLR).
SW1	push button	RP2354A RUN (reset).
SW2	push button	RP2354A BOOTSEL (QSPI_SS): hold while plugging in for the UF2 drive.
SW3	push button	PIC RD4 (10 kΩ pull-up), user input — not used by the firmware.
LED1	red LED	PIC RC5 via 330 Ω: heartbeat (blinks while the PIC firmware runs).
U4 + U5	RGB LED + LP5562	I²C LED driver at 0x30 (ADDR_SEL = GND, EN tied high); driven by `rgb R G B [pct]` since rp 1.1.1, brightness in % since 1.1.2 (internal clock, so OSC1 is not needed).
H1–H4	M2 holes	mounting, padded.

6 Firmware and host interface

6.1 Architecture

- **RP2354A** (`firmware/rp2354`, pico-sdk 2.1.0, `minus-rp2354` 1.1.2): USB CDC console, command parser, pulser PIO, gain mux, RP↔PIC link, and an ICSP programmer that flashes the PIC image embedded in the RP firmware.
- **PIC32AK** (`firmware/pic32`, XC-DSC 3.31, `minus-pic32` 1.1.0): clocks, op amps, ADC1/ADC2, SCCP trigger, DMA capture, pattern correction, link protocol 10.
- Update: `reboot dfu` (or SW2 at plug-in) → copy `minus_rp.uf2` to the RP2350 drive → `pic flash`. Prebuilt images are in the repository: `firmware/rp2354/build/minus_rp.uf2`, `firmware/pic32/build/minus_pic.hex`.

6.2 Command reference (USB console, one line per command)

Command	Description
`pe [hi [lo [in [dead]]]]`	Pulse-echo: arm the pulser on the next RDY rise, capture 4095 samples on input `in` (default 25), print header + samples; auto re-shot (≤ 8) if the sample clock locked slow. Defaults 200 ns / 500 ns / 25 / 27 ns.
`pulse [hi [lo [dead]]]`	One pulser shot now, no capture (scope check).
`gain [leg [u1 [u2]]]`	Set R_f leg 0–3 on both stages and unity bypass per stage; no argument: show.
`acq [div [samc [in [navg]]]]`	Capture without pulsing. `div`: trigger period in 5 ns (4 = 25 Msps, 10 = 20, 20 = 10); `samc` 0–7 sampling time; `in` input code; `navg` 1–16 summed conversions.
`pc [0|1]`	Fixed-pattern correction off/on; show last offsets.
`version`, `help`	Firmware, chip and unique ID; command list.
`ping`, `auto`, `stop`, `stat`	Link test (`PING n`→`PONG n`), periodic ping, counters.
`raw <text>`	Send a link line to the PIC and print the reply (e.g. `raw ID?`).
`pic id|flash|verify|erase|pins`	ICSP programmer for the PIC (pair 1, GPIO21/22/24).
`reset`, `reboot [dfu]`	PIC MCLR pulse; RP reboot / BOOTSEL.
`rgb R G B [pct]`	RGB LED colour, 0–255 per channel, LP5562 U5 on I²C at `pct` % brightness (0–100, default 25 = dim, scales the PWM); reply ends `(LP5562 0x30: ok)`.
`i2c`	I²C bus scan (found: 0x30).

Command	Description
`acqcpu`, `acqil`, `raw ADCBB`	Diagnostics / experiments (CPU-loop capture, two-channel interleave, ADC throughput).

Input codes: 0–15 = ADC1 PINSEL, 16–31 = ADC2 PINSEL + 16. Board 3: **25** AD2AN9 ADC node (default), 17 AD2AN1 OA2OUT, 0 AD1AN0 OA1OUT, 1 AD1AN1 LNA output (aliased wideband noise, see errata), 15/31 internal band gap, 14/30 internal 15/16 AVDD.

6.3 Data format

```
> pe
# acq n=4095 fill=164.7us fs=24.86Msps rp_fill=163us ... pulse-echo: pulse on RDY rise (+5V 200 / off 27 / GND 500
    ns),
# in=25 AD2AN9 (...), 40 ns/sample; gain leg 0 (Rf 2.2k) OA1 x1.00 (UGE) OA2 x3.20 = x3.2 (10.1 dB, + LNA); try 1
2019
2023
... (4095 lines, unsigned 12-bit codes, mid-scale ~2020)
# pulse fired, 1 shot(s)
```

Host software: the Python package in `python/library` wraps every command (one method each, replies parsed into objects), and the notebooks in `python/notebooks` walk through them step by step with the bytes on the wire. A check (`python -m minus.fwsync`) keeps the library in step with the firmware sources.

```
from minus import Minus # pip install -e python/library
dev = Minus() # finds /dev/ttyACM*, checks both firmware versions
dev.gain(2, 0, 0)
a = dev.pe() # a.samples (uint16), a.t_us, a.depth_mm(), a.fs_msps, a.shots
```

One-off commands from a shell: `python3 firmware/rp2354/tools/rpcli.py /dev/ttyACM0 "gain 2 0 0" "pe" -wait=2 > shot.txt`.

7 Application information

7.1 Getting a first A-line

1. Connect a 1–7 MHz single-element transducer to TX and RX (tee or the U.FL pair); plug USB-C.
2. Check: `version`, `raw ID`? (PIC answers), `ping`.
3. `gain 0 1 0` (≈ 11 dB) and `pe`; raise the gain until the echoes of interest use most of the ±2048 range without clipping.
4. Average several shots on the host for weak echoes, after aligning them on a strong echo (noise falls as $1/\sqrt{N}$: 11.6 dB for 8 shots[M]).

7.2 Choosing the pulse

A unipolar pulse of length t has a spectrum $\propto |\sin(\pi f t)|$: strongest at f_c for $t = 1/(2f_c)$ and nulled at $t = 1/f_c$. The measured curve (12 points below 150 ns) has its maximum at t_{hi} = 113 ns and its minimum near 250 ns — both about 48 ns earlier than the ideal 155 ns / 310 ns at 3.22 MHz. The effective +5 V pulse is therefore t_{hi} + ≈ 48 ns: during the 27 ns dead time nothing pulls the output down (it stays at +5 V on the cable capacitance) and the driver turn-on/turn-off delays add the rest. Below ≈ 25 ns the driver no longer reaches full swing (13 ns gives almost no echo). For this probe `pe 100` gives 1.9 times the echo amplitude of the 200 ns default; the plateau is 75–130 ns. The GND clamp length (0–2 µs) changes neither the echo amplitude nor the 8.2 µs ring-down much: the ring-down is the transducer's own; the clamp mainly defines the end state before the output is released.

7.3 Limitations

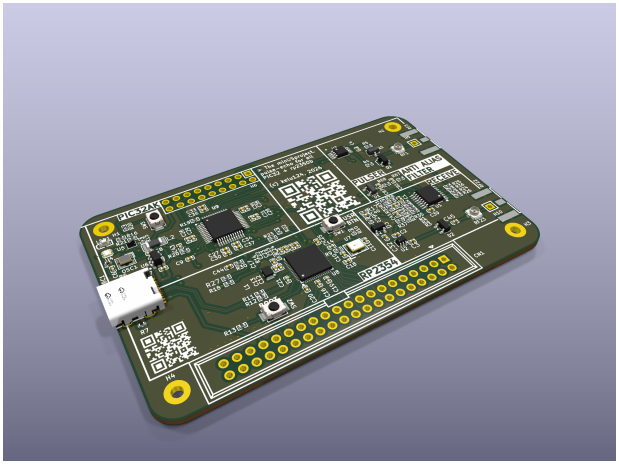
- Throughput is limited by the 115 200 Bd RP↔PIC link: 0.88 s per shot, i.e. 1.14 shots/s (the capture itself takes 165 µs).
- No time-gain compensation yet: the gain is fixed during a capture.
- 5 V excitation only: echoes from deep or attenuating targets need averaging.

8 Known issues (errata)

ID	Issue and workaround
E1	**TX at +5 V during power-up.** GPIO9 has no pull-up; the RP2350 pad default pull-down turns Q1 on until the firmware idles the pins (a few ms). Fix: 10 kΩ pull-up on GPIO9, 10 kΩ pull-down on GPIO8. The net names PWM_H/PWM_L are swapped vs function.
E2	**ADC slow lock.** The 32 ns conversion on 20 ns triggers sometimes locks to 40/60/60 ns. Detected on the PIC since 0.1.25 (status `slow`); `pe` and `acq` re-shoot automatically (≤ 8).
E3	**Sample-comb phase** varies over one sample period from shot to shot (39 ns p-p, 11.3 ns rms, independent shots), and the comb slips by a whole sample during 14–31 % of captures (more often later in the capture; §4.6). Align on the echo of interest before averaging. Root cause (SCCP/ADC clock-domain start) not yet fixed.
E4	**Period-4 fixed pattern** on external ADC inputs (10.5 LSB rms). Removed in firmware (`pc`); source of the coupling not yet found.
E5	**Interference lines** at 2.72 MHz (in band) and 0.49 MHz entering at the front end; up to half the in-band noise at high gain. Source unknown.
E6	**LNA output tap (input 1)** reads 26 mV rms of flat, aliased noise that does not reach OA1OUT: GHz-wide LNA noise or an oscillation folded by the ADC sample-and-hold. Not a valid measurement point; to check with a fast scope.
E7	**RGB LED** — *fixed in rp 1.1.1*: `rgb` now drives the LP5562 over I²C (the WS2812 driver on GPIO10 was for the devkit).
E8	`reboot dfu` occasionally restarts the application instead of BOOTSEL; use SW2 at plug-in.
E9	U3 is fitted as MIC4427YMM (TC4427 out of stock); design files still list TC4427AEUA713.
E10	Internal 15/16 AVDD channel reads 3480 instead of 3840 codes; internal references need SAMC ≥ 3.
E11	**TX and RX are separate nets**: a single-element probe needs an external tee (a 0 Ω TX–RX link is planned for the next revision).

9 Mechanical

Outline	85.65 × 54.03 mm
Thickness	1.6 mm, 4 copper layers
Mounting	4 × M2 (2.2 mm, padded)
Components	120 footprints, 39 R, 47 C
Main ICs	RP2354A (QFN-60), PIC32AK1216GC41048 (TQFP-48), BGA2817 (SC-70-6), 74HC4052 (TSSOP-16), TC4427/MIC4427 (MSOP-8), AP2112K (SOT-23-5), LP5562 (DSBGA-12)
Design files	`hardware/` (KiCad), JLC outputs in `hardware/production/`



10 License and resources

- Source, design files, firmware, bench data and this datasheet: github.com/kelu124/minus.
- Hardware (`hardware/`): TAPR Open Hardware License v1.0. Firmware and scripts (`firmware/`, `python/`, bench scripts): GNU GPL v3.0 or later. Documentation, this datasheet and the bench data: CC BY-SA 4.0. Full texts in `LICENSES/`; third-party parts (EasyEDA 3D models, Pico SDK, Microchip DFP) keep their own licenses (`LICENSE.md`).
- **Not a medical device.** For research, education and non-destructive testing only.

11 Revision history

Rev	Date	Change
0.1	2026-11-19	First release: board 3 bring-up, firmware rp 0.1.34 / pic 0.1.25, measurements of session 11.
0.2	2026-11-19	Board named v1.1; firmware rp 1.1.2 / pic 1.1.0 (LP5562 `rgb` with brightness, E7 fixed); Python library + notebooks; E3 sample-comb phase study (400 shots); licenses and repository links; Annex A test transducer.

Annex A — Test transducer

Every [M] value in this datasheet was taken with the same single-element piezo probe (“BiVi piezo”, 3.3 MHz nominal), on TX and RX. Its one-port reflection was measured by the owner with a NanoVNA (`datasheet/piezo_test/BiViPiezo.s1p`: 606 points, 2.0–5.6 MHz, S_{11} re/im, 50 Ω). The values below come from `datasheet/piezo_test/analyze_s1p.py`. The measurement is at the VNA port, so it includes any cable or adapter.

Parameter	How	Value
Return-loss dip 1	minimum of $\lvert S_{11}\rvert$	3.31 MHz, 17.5 dB, Z = 55 − j13 Ω
Return-loss dip 2	second minimum	4.16 MHz, 15.5 dB, Z = 58 + j16 Ω
Return loss between the dips	worst point between them	9.8 dB at 3.78 MHz
Return loss ≥ 10 dB	(VSWR ≤ 1.92)	3.12–3.74, 3.83–4.38 MHz
|Z| over 3.0–4.4 MHz		26–83 Ω
Impedance at 3.30 MHz		58 Ω, −13°
Conductance peak	max Re(1/Z)	3.77 MHz
Resistance peak	max Re(Z)	4.32 MHz
Phase zero crossings		3.22, 3.74, 4.27 MHz

The probe looks **electrically matched to 50 Ω**: |Z| stays within 26–83 Ω across 3–4.4 MHz, the response loops round the centre of the Smith chart, and away from resonance the susceptance is inductive. A bare ceramic would be capacitive there, so a Butterworth–Van Dyke fit of the element itself does not apply. The double dip is typical of a matched, damped probe. The acoustic echo band measured through the board (electrical characteristics, “Echo −6 dB band”: 2.88–3.55 MHz, peak 3.37 MHz) sits on the lower dip. The 200 ns unipolar pulse, the two-way transducer response and the RX anti-alias filter all weight the echo spectrum towards lower frequencies.

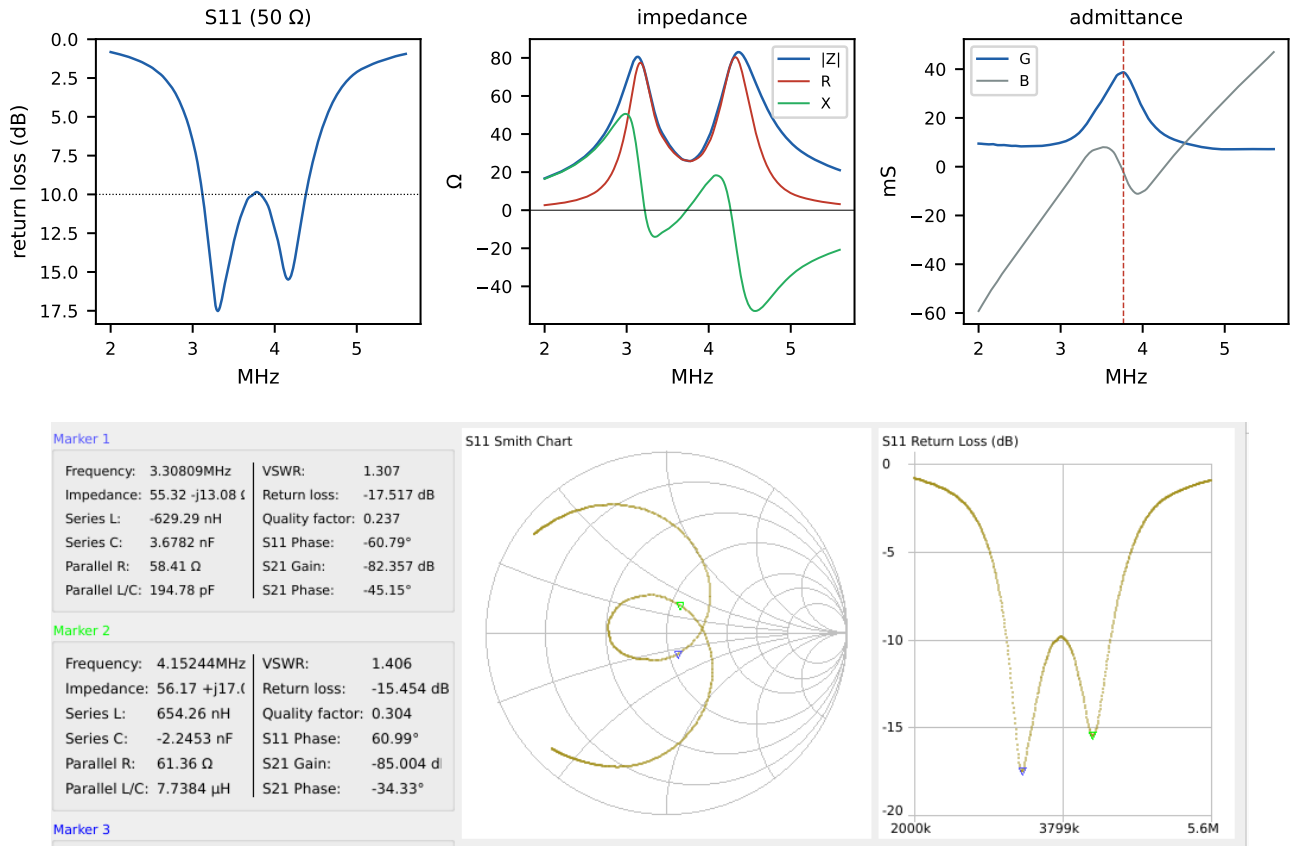


Figure 10: Test transducer, S_{11} from `BiViPiezo.s1p`. Top: return loss, impedance (|Z|, R, X), admittance (G, B; dashed = conductance peak). Bottom: the NanoVNA screen as measured (markers at the two return-loss dips).